REMARKS

In response to the Office Action dated August 21, 2007, no amendments are made. Claims 1-5 were previously cancelled without prejudice. Claims 6-16 are active. Claims 6 and 13 are the only independent claims.

Applicants appreciate the Examiner's indication of allowable subject matter in claims 15 and 16, at pages 14 and 15 of the Office Action. Claims 15 and 16 are objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim.

Claims 6-9 are rejected under 35 U.S.C. § 102(b) as being anticipated Shoji (U.S. Patent 4,670,670). Applicants traverse this rejection.

Claims 13-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kaenel et al. (U.S. Patent 5,682,118). Applicants traverse this rejection.

Claims 6-9 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang (U.S. Patent Publication 2004/0070440) in view of Forbes et al. (U.S. Patent 6,456,157). Applicants traverse this rejection.

Claims 10 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Forbes and further in view of Bowden (U.S. Patent 4,427,935). Applicants traverse this rejection.

Independent claim 6 recites, in part, "a substrate potential control circuit for **controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value** that is

sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit.."

Similarly, independent claim 13 recites, in part, "a target saturation current value of the MOS transistors that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage, is set in the power supply voltage control circuit; and the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit **so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value.**"

As an illustrative and non-limiting example of claim 6, please note Expression 2 in the application which indicates delay time (τ) as a function of: load capacitance (C) times power supply voltage (Vdd) divided by saturation current (Ids). Further, please note Expression 3 in the application which indicates saturation current (Ids) as a function of multiple variables including threshold voltage (Vt). Additionally, please note Expression 1 which indicates threshold voltage (Vt) as a function of multiple variables including substrate voltage (Vb). For convenience, these expressions are provided below:

(Expression 1) $Vt = Vto+\gamma(\sqrt{(\alpha-Vb)})$

(Expression 2) $\tau = C \cdot Vdd/Ids$

(Expression 3) $Ids = (1/2)\mu Cox(W/L)(Vdd-Vt)^2$

In summary, the substrate potential (Vb) controls the threshold voltage (Vt) via Expression 1, then the threshold voltage (Vt) controls the saturation current (Ids) via Expression 3, and finally the saturation current (Ids) controls the delay time (τ) via Expression 2. Of course, the delay time (τ) is inversely proportional to the operation speed of the main circuit.

Additionally, as an illustrative and non-limiting example of claim 6, please note substrate potential control circuit 1n including current-voltage conversion circuit 1n-3 in FIG. 5, and the associated written description in the application (especially page 19, line 25 to page 20, line 12).

Please note that claim 6 is rejected under 35 U.S.C. § 102(b) as being anticipated Shoji, **and** is also rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang (U.S. Patent Publication 2004/0070440) in view of Forbes et al. (U.S. Patent 6,456,157).

As is well known, anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). The elements must be arranged as required by the claim. *In re Bond*, 910 F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Additionally, in order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *In re Rokya*, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974). Further, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation.

The Office Action, at page 3, asserts that Shoji, at FIG. 1, discloses all of the limitations of claim 6. Specifically, the Office Action asserts that the circuit of FIG. 1 of Shoji is connected "exactly" as shown in the substrate potential control circuit of FIG. 5 of the instant application. However, the substrate potential control circuit of FIG. 5 of the instant application contains a constant current source (at the top left), and FIG. 1 of Shoji does **not** contain any constant

current source. Additionally, the substrate potential control circuit of FIG. 5 of the instant application contains an operational amplifier connected to the source and drain of the transistor, and FIG. 1 of Shoji does **not** contain any similarly connected operational amplifier. Thus, FIG. 1 of Shoji is very different from FIG. 5 of the present application.

Shoji, at the abstract, merely states that the, "threshold voltage of a CMOS circuit is stabilized by a feedback loop which responds to variations in threshold voltage of a reference FET to provide a backbias voltage to **readjust the threshold voltage** of a second FET." In other words, Shoji is merely directed towards controlling the threshold voltage of a second FET.

Thus, Shoji does not teach or suggest "controlling the substrate potential of a MOS transistor in the main circuit so that **an actual saturation current value of the MOS transistor is equal to a target saturation current value**" as recited by claim 6.

Additionally, the Office Action, at page 6, asserts that Tang, at element 100 in FIG. 1, discloses the substrate potential control circuit of claim 6. Tang, at paragraph [0010], merely discloses a bias voltage (Vbs) that is fixed or variable.

However, Tang does not teach or suggest "controlling the substrate potential of a MOS transistor in the main circuit so that **an actual saturation current value of the MOS transistor is equal to a target saturation current value**" as recited by claim 6.

Additionally, the other cited publications (Kaenel, Forbes, and Bowden) do not remedy the deficiencies of Shoji and Tang.

Thus, Applicants submit that independent claim 6 is allowable for at least the foregoing reasons. Additionally, Applicants submit that independent claim 13 is allowable for similar reasons.

Under Federal Circuit guidelines, a dependent claim is allowable if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987).

Thus, as independent claims 6 and 13 are allowable for the reasons set forth above, it is respectfully submitted that dependent claims 7-12 and 14-16 are allowable for at least the same reasons as their respective base claims.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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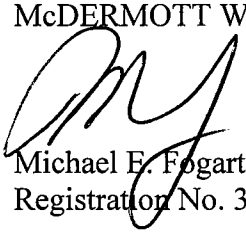

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